Jung et al. Nano Convergence (2015) 2:11
DOI 10.1186/s40580-015-0042-x

Nano Convergence
a SpringerOpen Journal

REVIEW Open Access

Interface engineering for high performance graphene electronic devices

Dae Yool Jung†, Sang Yoon Yang†, Hamin Park, Woo Cheol Shin, Joong Gun Oh, Byung Jin Cho* and Sung-Yool Choi*

Abstract

A decade after the discovery of graphene flakes, exfoliated from graphite, we have now secured large scale and high quality graphene film growth technology via a chemical vapor deposition (CVD) method. With the establishment of mass production of graphene using CVD, practical applications of graphene to electronic devices have gained an enormous amount of attention. However, several issues arise from the interfaces of graphene systems, such as damage/unintentional doping of graphene by the transfer process, the substrate effects on graphene, and poor dielectric formation on graphene due to its inert features, which result in degradation of both electrical performance and reliability in actual devices. The present paper provides a comprehensive review of the recent approaches to resolve these issues by interface engineering of graphene for high performance electronic devices. We deal with each interface that is encountered during the fabrication steps of graphene devices, from the graphene/metal growth substrate to graphene/high-k dielectrics, including the intermediate graphene/target substrate.

Keywords: Graphene; Interface engineering; Transfer; Delamination; Mobility; Doping; Hysteresis; Substrate effect; Dielectric; Transistor

1 Introduction

Graphene has received massive attention as a promising new material for application to electronic and optoelectronic devices because of its superior and unique electrical, optical, and mechanical properties [1-10]. In the early stage of graphene research, high quality graphene obtained by mechanical exfoliation [1-8] of graphite facilitated fundamental studies on the outstanding properties of graphene, triggering explosive research on the application of graphene to various fields [11-15]. However, the application of graphene to real-world devices requires a scalable synthesis technique to overcome the limited quantity and size of mechanically exfoliated graphene. Graphene synthesis by chemical vapor deposition (CVD) [16-25] is currently the most widely adopted technique for the scalable production of single layer graphene, up to a size of 30 inches [19]. Although large-scale, high-quality graphene is now available, the realization of high performance graphene devices is still challenging. Specifically, devices fabricated from CVD-grown graphene have not yet shown the level of performance that was anticipated upon the emergence of graphene [26-29]. While the degradation of the performance of graphene devices can be attributed to many factors, the significant issue of the interfaces where graphene interacts with the neighboring materials warrants extensive consideration [30-35]. Due to the one-atom-thick, two-dimensional (2D) characteristic of graphene, its electrical properties are directly affected by the interaction of the graphene surface with adjacent materials.

The purpose of this review is to shed light on the importance of interface engineering through the entire fabrication process of graphene devices from several recent reports on graphene transfer and graphene electronic devices. In this review, we start from novel transfer techniques via direct delamination of graphene from a metal growth substrate, which is closely relevant to the interface control in a graphene/growth (or graphene/target) substrate. After the transfer process, graphene forms an interface with a target substrate, which also influences

* Correspondence: sungyool.choi@kaist.ac.kr; elebjcho81@kaist.ac.kr
†Equal contributors
Graphene Research Center, Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon 305-701, Republic of Korea

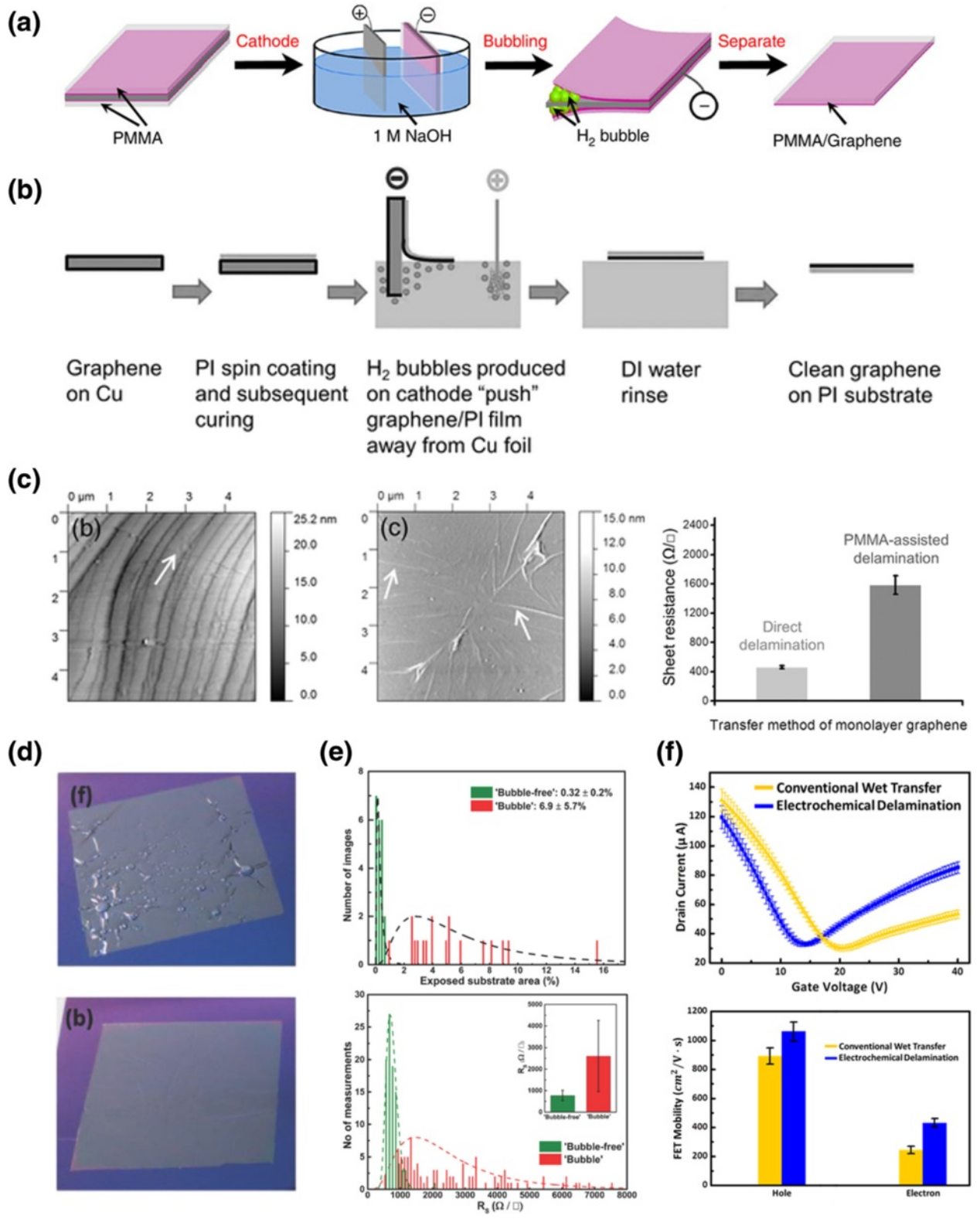

Figure 1 (See legend on next page.)

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Figure 1 Electrochemical delamination of graphene. a, Illustration of electrochemical delamination of graphene from Pt foil with PMMA sacrificial layer. Reproduced with permission [46]. Copyright 2012, Nature Publishing Group. **b**, Illustration of direct delamination of graphene onto polyimide substrate without PMMA sacrificial layer. Reproduced with permission [47]. Copyright 2014, John Wiley and Sons. **c**, AFM images of transferred graphene on polyimide without sacrificial layer (left) and with PMMA sacrificial layer (middle) via electrochemical delamination. Sheet resistance of monolayer graphene on polyimide transferred by the direct delamination method and the PMMA-assisted delamination method (right). Reproduced with permission [47]. Copyright 2014, John Wiley and Sons. **d**, 'Bubble' (top) and 'bubble-free' (bottom) delaminated and transferred PMMA/graphene stack on oxidized silicon wafer. Reproduced with permission [48]. Copyright 2014, John Wiley and Sons. **e**, Histograms of percentage of exposed substrate area (top panel) and sheet resistance (bottom panel) for films delaminated using the 'bubble-free' (green) and 'bubble' (red) methods. Inset of bottom panel: Sheet resistance of samples obtained via 'bubble-free' and 'bubble' delamination. Reproduced with permission [48]. Copyright 2014, John Wiley and Sons. **f**, Transfer characteristics (I_d-V_g) of fabricated graphene FET (top panel) and FET mobility (bottom panel) of which graphene are transferred via 'conventional wet transfer' (yellow) process and 'electrochemical delamination' (blue) process.

the charge carrier transport of graphene. Hence, we discuss the substrate effects and the choice of an optimum substrate for high performance graphene devices. Finally, when graphene is transferred intact onto the target substrate, it is necessary to consider other interfaces that are created by the integration of graphene with other electronic components such as gate dielectrics. These interfaces also give rise to challenging issues related to the chemical inertness of the graphene surface and the wettability/interfacial adhesion. The last topic covers novel strategies to integrate uniform, ultrathin gate dielectrics on the graphene surface to guarantee high performance of graphene devices.

2 Review

2.1 Transfer techniques: interfaces at graphene/metal growth substrate and graphene/target substrate

Since large-area graphene films are mainly synthesized on catalytic metal substrates [16-23], we first should consider the interface between graphene and the catalytic metal substrate. To apply CVD-grown graphene to electronic devices, graphene must be isolated from this interface and delivered to a target dielectric substrate. The most common method for graphene transfer has been poly(methyl methacrylate) (PMMA) film-assisted transfer [36-39], which involves wet etching of the metal substrate and water-mediated delivery of graphene to the target substrate. Drawbacks of this method include possible oxidation of graphene due to the strong oxidation power of metal etchants [19] and contamination of graphene by etching residues such as ionic impurities from the etchant [40-42] and metallic residues from incomplete etching [41]. In addition, polymeric residues [31-33] after PMMA removal are another source of contamination of graphene. These residues directly affect the electrical properties of graphene, resulting in significant degradation of the performance of graphene devices [31-33,43]. For these reasons, metal-etching-free transfer by delamination of graphene from the metal substrate has been pursued as an alternative, non-destructive means of realizing clean transfer of graphene.

2.1.1 Electrochemical delamination/transfer of graphene: physical weakening of the graphene/metal interface

One strategy for direct delamination of graphene is physical weakening of the interfacial interactions between graphene and the metal growth substrate. Figure 1a schematically illustrates the electrochemical delamination (ECD) of graphene in which hydrogen (H_2) bubbles generated by the electrolysis of water are utilized as a tool for physical weakening of the graphene/metal interface [44]. The electrochemical cell employed for the delamination consists of a PMMA/graphene/metal substrate (cathode, biased negatively) and glassy carbon or noble metal with low reactivity (anode, biased positively), which are placed in an aqueous electrolyte solution, such as $K_2S_2O_8$ [44], NaOH [45,46], Na_2SO_4 [47] or NaCl [48,49]. Under applied bias, electrolysis of water at the cathode induces the generation and penetration of H_2 bubbles along the interface between PMMA/graphene and the metal substrate, resulting in gradual separation of PMMA/graphene from the metal substrate. Note that partial etching of a copper (Cu) or nickel substrate can occur by the electrolyte during the ECD process, and this can be suppressed by the choice of an appropriate electrolyte such as Na_2SO_4 [47]. This method is highly useful for systems where graphene is synthesized on chemically inert, noble metals such as platinum [46], ruthenium [50] or iridium [51], because etchants for corresponding metals are rarely available. Wang et al. reported the application of the ECD process for the direct transfer of graphene to a flexible polyimide substrate by depositing the target polyimide substrate directly onto the graphene/metal growth substrate, instead of PMMA, where no water-mediated graphene delivery to a foreign target substrate is required (Figure 1b) [47]. Elimination of the conventional use of a sacrificial PMMA enables the production of nearly residue-free graphene with a low density line defects (ripples and wrinkles), yielding flexible, transparent conducting films with low sheet resistance (~459 Ω/sq for single layer graphene, ~49 Ω/sq for multilayer graphene) (Figure 1c).

In the ECD based transfer method, one critical issue is mechanical damage of graphene by H_2 bubbles. These

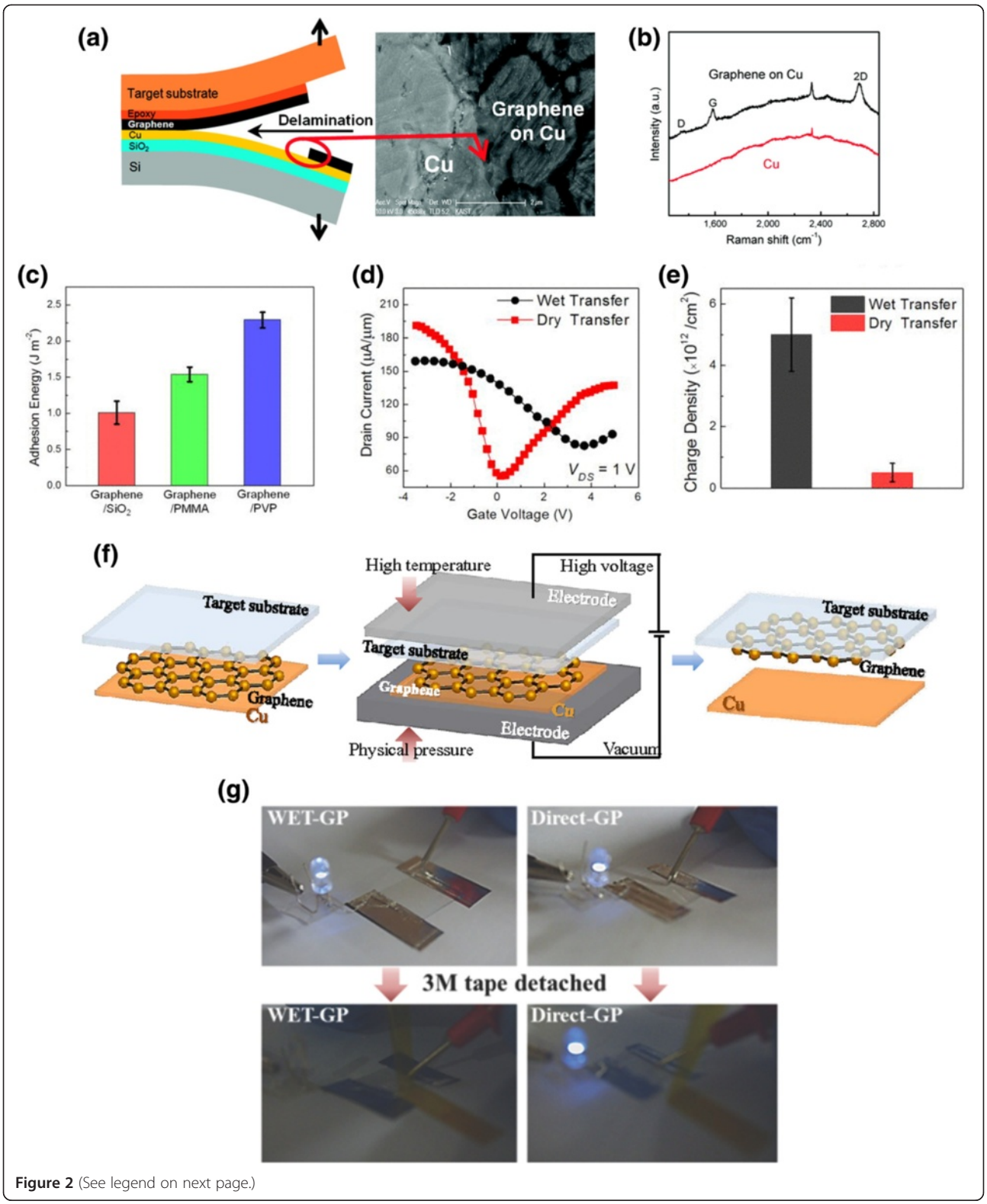

Figure 2 (See legend on next page.)

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Figure 2 Dry transfer using difference of adhesion energy between graphene/metal and graphene/target substrate. a, Illustration of graphene transfer using the mechanical delamination process and high-magnification SEM image of boundary of delamination. Reproduced with permission [53]. Copyright 2012, American Chemical Society. **b**, Raman spectra of the graphene-delaminated bare copper (the lower spectrum) and of the graphene-covered copper (the upper spectrum). Reproduced with permission [53]. Copyright 2012, American Chemical Society. **c**, Directly measured adhesion energy of graphene to neighboring materials (SiO_2, PVP, and PMMA). Reproduced with permission [54]. Copyright 2013, AIP Publishing LLC. **d**, Transfer characteristics (I_{DS}-V_{GS}) of the graphene FETs fabricated using conventional wet transfer (black) method and dry transfer with PVP adhesive layer (red). Reproduced with permission [54]. Copyright 2013, AIP Publishing LLC. **e**, Charge density of the graphene FETs fabricated using conventional wet transfer (black) method and dry transfer with PVP adhesive layer (red). Reproduced with permission [54]. Copyright 2013, AIP Publishing LLC. **f**, Schematic description of the mechano-electro-thermal (MET) delamination process of graphene. Reproduced with permission [55]. Copyright 2014, John Wiley and Sons. **g**, Strong mechanical stability of MET graphene via demonstration of LED electrical circuit based on graphene/PET film using repeated detaching of 3M tape. Reproduced with permission [55]. Copyright 2014, John Wiley and Sons.

bubbles can directly damage graphene during the delamination process by considerable turbulence or can result in cracks (or voids), ripples, and wrinkles due to the trapped H_2 between the graphene and the target substrate (upper panel in Figure 1d) [45,48]. Such transfer-induced damage or defects severely degrade the electrical properties of graphene devices in terms of mobility and sheet resistance. To eliminate or reduce the mechanical damage caused by H_2 bubbles, Cherian et al. developed a 'bubble-free' delamination/transfer method by exploiting the electrochemical reduction (dissolution) of adventitious cuprous oxide (Cu_2O) sandwiched between graphene and a Cu substrate as a tool for weakening of that interface [48]. Reduction of interfacial Cu_2O occurred at an optimum potential lower than that required for the generation of H_2 bubbles. This method resulted in uniform adherence of PMMA/graphene to the target substrate (lower panel of Figure 1d) and the resulting transferred graphene film exhibited a negligible amount of voids (upper panel of Figure 1e) and high uniformity of electrical properties (lower panel of Figure 1e). Damages in graphene by the generation of H_2 bubbles can be also alleviated with a simple plastic-frame-assisted method [45]. In a previous study we performed ECD-graphene transfer using a similar method to the plastic-frame-assisted approach to compare the quality of the transferred graphene by the ECD method with that by the conventional PMMA-assisted wet method in terms of the characteristics of a field-effect transistor (FET). Experimental details are described in [52]. We found that the electrical characteristics of ECD-graphene FETs reflected the effective suppression of p-doping (reduced Dirac point) and enhanced FET mobility with symmetrical electron–hole conduction (Figure 1f).

2.1.2 Dry transfer of graphene: difference of adhesion energy between graphene/metal and graphene/target substrate interfaces

Graphene transfer based on direct delamination can also be achieved by exploiting the difference in adhesion energies between graphene/metal and graphene/target substrate interfaces [53,54]. The basic concept of this approach is illustrated in Figure 2a: An adhesive interface is formed between a graphene/metal substrate and a target substrate, and then the two substrates are separated under tensile loading by double cantilever beam fracture testing [53]. The Raman spectra in Figure 2b indicate that application of an appropriate adhesive layer enables mechanical delamination of graphene from the Cu substrate. As shown in Figure 2c, Shin et al. measured the adhesion energy of graphene to various adhesive layers (or target substrates) and found that a graphene/poly(vinyl phenol) (PVP) system exhibited the highest adhesion energy ($2.31 \pm 0.11\ Jm^{-2}$), higher than that of a graphene/Cu system ($0.72 \pm 0.07\ Jm^{-2}$) [53]. This indicates that PVP can act as an appropriate adhesive that induces successful delamination and transfer of graphene from Cu to a target substrate [54]. Because a wet process is excluded, this transfer method is called 'dry transfer'. As mentioned in Section 2.1, advantages of the delamination/transfer method include the restoration of charge neutrality and symmetrical electron–hole conduction of graphene, which are usually degraded by a metal etching process in the conventional wet transfer approach. Figures 2d and 2e show p-doping suppression and enhanced electron current modulation of dry-transferred graphene FETs, in comparison to graphene FETs prepared using either conventional wet transfer or ECD transfer (Figure 1f) [54]. These enhancements obtained with dry transfer are attributed to the absence of opportunity for graphene to be contaminated by ionic impurities (from either the electrolyte or metal etchant) and metallic residues (from incomplete etching of the metal substrate).

Jung et al. recently exploited a mechano-electro-thermal (MET) process to induce delamination and dry transfer of graphene from a Cu substrate directly to various substrates such as glass, PET, and PDMS (Figure 2f) [55]. The key aspect of this method is to form strong and ultra-conformal contact between graphene/Cu and a target substrate by applying high temperature, physical pressure, and high voltage simultaneously to the Cu

foil/graphene/target substrate stack. Graphene is transferred to the target substrate simply by peeling the Cu foil off after the MET process. No polymeric carriers or adhesives are used in this approach. Most importantly, graphene transferred by the MET process exhibited outstanding interfacial adhesion with the target substrate as a result of the ultra-conformal contact formation: the mechanical adhesion stability of graphene is maintained even after several cycles of tape detaching tests, as shown in Figure 2g.

2.1.3 Direct delamination/transfer of graphene with high degree of freedom

Recently, Yang et al. reported that the combination of pretreatment of graphene/Cu substrate with the well-known transfer printing technique allows clean delamination and transfer of graphene, which can also endow the graphene transfer process with a high degree of freedom (Figure 3a) [56]. Delamination of graphene is induced by the adsorption of a water soluble polymer (poly(vinyl alcohol) in this case) on the graphene growth substrate, followed by the

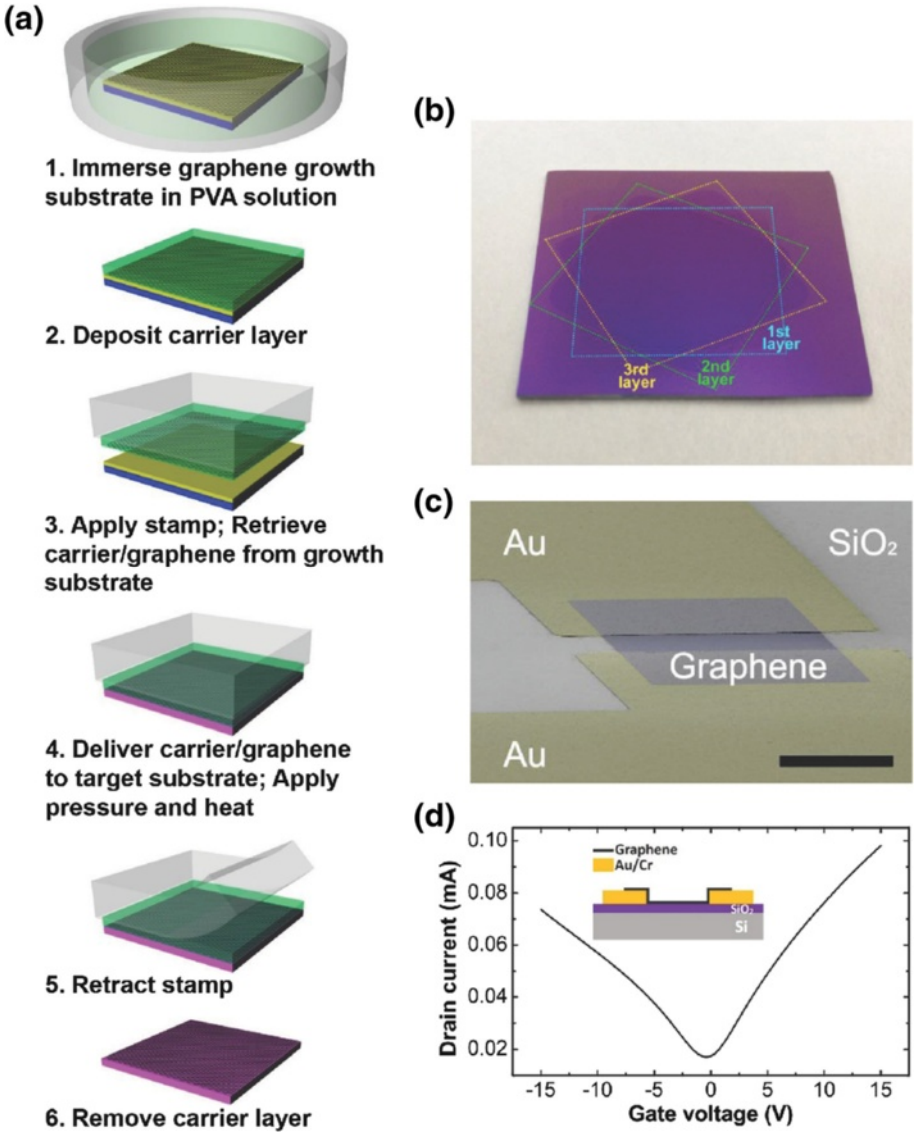

Figure 3 Direct delamination and transfer of graphene using transfer printing method. a, Schematic illustration of direct delamination and transfer of graphene with PVA carrier layer. Reproduced with permission [56]. Copyright 2014, John Wiley and Sons. **b**, Three-layered graphene fabricated by layer-by-layer stacking in a deterministic manner on oxidized silicon wafer. Reproduced with permission [56]. Copyright 2014, John Wiley and Sons. **c**, False-color scanning electron microscope image of transferred graphene on gold electrodes. Reproduced with permission [56]. Copyright 2014, John Wiley and Sons. **d**, Transfer characteristics of bottom-contact graphene FET with transferred graphene on top of gold source/drain electrodes. Reproduced with permission [56]. Copyright 2014, John Wiley and Sons.

Table 1 Summary of graphene transfer methods

	Graphene/metal separation	Graphene delivery to target substrate	Graphene isolation (its supporting layer)	Degree of freedom	Renewability of metal substrate	Origin of graphene defects[c]	References
Conventional polymer-assisted, wet transfer	Metal etching	Water-mediated scooping	O (PMMA)	High	X	Metal etching process	[36-39]
Electrochemical delamination/transfer	Electrochemical delamination by H_2 bubbles	Water-mediated scooping	O (PMMA)	High	O	H_2 bubbles	[44-49,52]
Adhesive-assisted dry transfer	Mechanical delamination by adhesive	Direct transfer[a]	X (NA)[b]	Very low	O	Incomplete delamination	[53,54]
Dry transfer with MET process	Mechanical delamination by MET process	Direct transfer[a]	X (NA)[b]	Low	O	Incomplete delamination	[55]
Transfer printing via direct delamination	Mechanical delamination by pre-treatment	Stamp-mediated printing	O (PVA)	High	O	Incomplete delamination	[56]

[a]Delamination and transfer of graphene occur simultaneously. [b]Supporting layer is not applicable. [c]Defects include damage or contamination of transferred graphene.

formation of a carrier layer using the same polymer. Because the delaminated graphene can exist in an isolated state on an elastomeric support during this transfer process (step 3 in Figure 3a), this transfer method allows the graphene to form effective junctions with itself (layer-by-layer stacking, Figure 3b) or with other electronic components (graphene on source/drain electrodes, Figures 3c and 3d), indicating the high degree of freedom and the resulting versatility of the developed method. Table 1 provides a summary of graphene transfer methods.

2.2 Interface engineering of graphene/target substrate

2.2.1 Modification of graphene/target substrate interface

After the transfer process, graphene makes contact with a target substrate. Thermally grown silicon dioxide (SiO_2) has been widely used as a target substrate from the early stage of graphene research due to its commercial availability, relatively small surface roughness, and the clear visibility of single layer graphene on it at a specific thickness of SiO_2 (c.a. 90 or 300 nm) [57,58]. However, when graphene is placed on a SiO_2 substrate, the performance of graphene FETs is considerably degraded by the substrate effects [59-66]. The substrate effects, with respect to the mobility limitation of graphene, include the scattering of carriers in graphene by charged impurities [64] and surface phonons [60]: the FET mobility of graphene/SiO_2 is several orders of magnitude lower than that of suspended graphene devices [60,61]. In addition, the adsorbed water molecules by silanol (SiOH) groups at the graphene/SiO_2 interface result in unintentional p-doping of graphene [67-69] and hysteresis of graphene FETs [66,70,71].

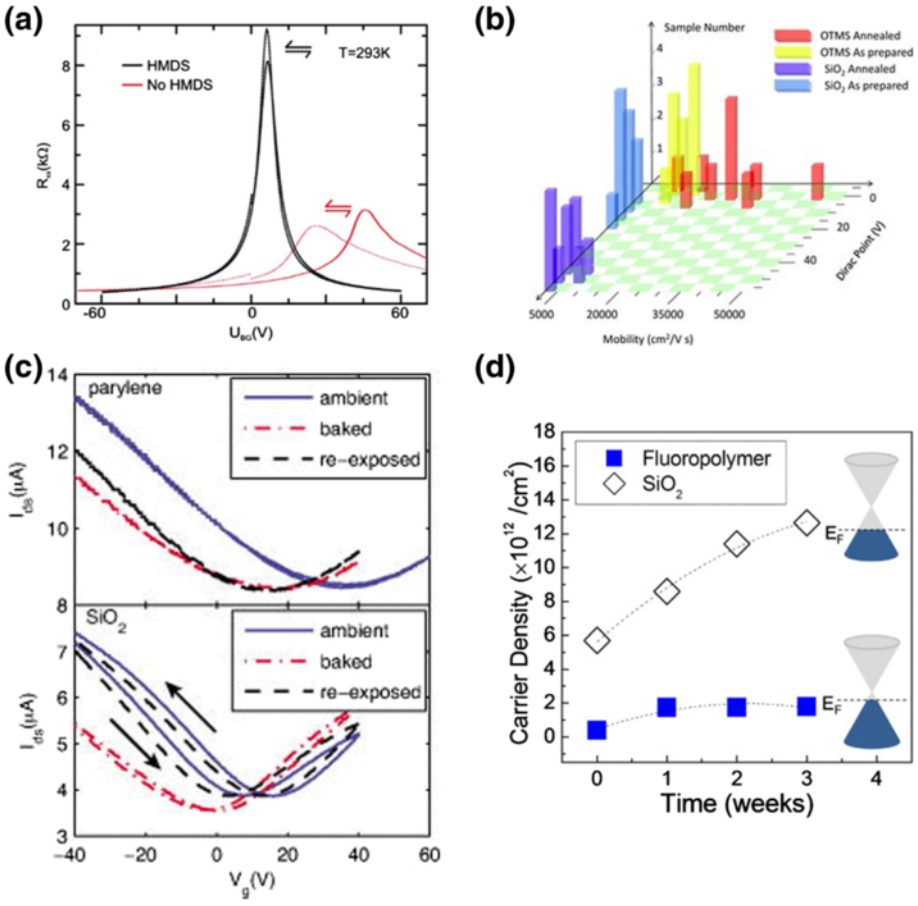

Figure 4 Passivation of target substrate for transferred graphene. a, Field effect measurement at T = 293 K for graphene on HMDS (black) and for graphene on bare SiO_2 (red). Reproduced with permission [73]. Copyright 2010, American Chemical Society. **b**, Histogram of mobility and the Dirac point of different graphene FETs on bare SiO_2/Si and on OTMS-modified SiO_2/Si substrates at room temperature under ambient conditions. Reproduced with permission [77]. Copyright 2011, John Wiley and Sons. **c**, Transfer characteristics (I_{ds}-V_g) for a typical parylene gated FET in air, baked at 400 K in vacuum, and in air 30 min after baking (top panel). Drain-source current versus back-gate voltage for silicon oxide devices in air, baked at 400 K in vacuum, and in air 30 min after baking (bottom panel). Reproduced with permission [78]. Copyright 2009, AIP Publishing LLC. **d**, The change in carrier density in graphene on different surface (fluoropolymer and SiO_2) with elapse of time in an air ambient. Reproduced with permission [79]. Copyright 2011, AIP Publishing LLC.

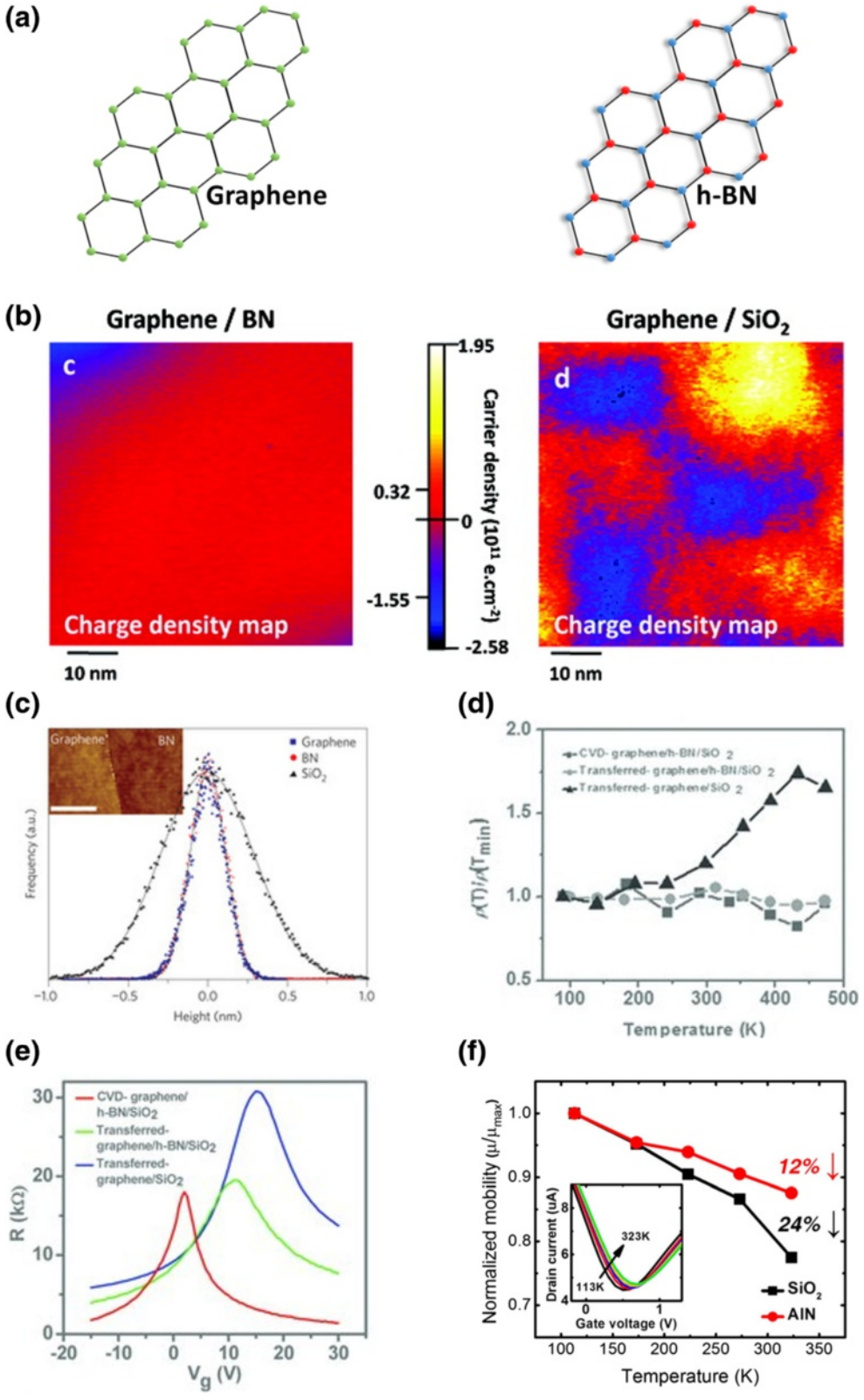

Figure 5 (See legend on next page.)

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Figure 5 h-BN and AlN as supporting substrates for graphene. a, Atomic structure of graphene and hexagonal boron nitride. **b**, Charge density map of graphene/BN and graphene/SiO_2. Reproduced with permission [97]. Copyright 2011, American Chemical Society. **c**, Histogram of the height distribution (surface roughness) measured by AFM for SiO_2 (black triangles), h-BN (red circles) and graphene-on-BN (blue squares). Reproduced with permission [92]. Copyright 2010, Nature Publishing Group. **d**, Temperature dependences of the resistivity at V_g-V_{Dirac} = 10 V for CVD-grown graphene/h-BN, mechanically transferred graphene/h-BN, and graphene on SiO_2. Reproduced with permission [98]. Copyright 2013, John Wiley and Sons. **e**, Resistance versus applied gate voltage for CVD-grown graphene/h-BN, mechanically transferred graphene/h-BN, and graphene on SiO_2. Reproduced with permission [98]. Copyright 2013, John Wiley and Sons. **f**, Normalized change in carrier mobility with temperature for graphene FETs on AlN and SiO_2 substrates. Reproduced with permission [99]. Copyright 2014, AIP Publishing LLC.

Passivation of the SiO_2 surface with a hydrophobic buffer layer has been suggested as an effective route to improve the interface properties of SiO_2. Two types of buffer layers have been studied for this purpose: self-assembled monolayers (SAMs) [72-77] and thin polymer layers [78,79]. Lafkioti et al. reported that the intrinsic charge neutrality of graphene was recovered and the hysteresis of graphene FETs was dramatically reduced by modifying the graphene/SiO_2 interface with hexamethyldisilazane (HMDS) (Figure 4a) [73]. Wang et al. also observed similar phenomena with alkyl-terminated SAM. In both cases, the mobility of graphene increased several-fold, as compared to devices on bare SiO_2. Representative results for alkyl-SAM are shown in Figure 4b [77]. The hydrophobic treatments eliminate SiOH groups and the adsorbed water molecules at the graphene/SiO_2 interface, resulting in suppression of p-doping in graphene. In addition, the scattering induced by charged impurities and surface polar phonons can be screened due to the increase of the graphene-substrate distance via interface modification with HMDS or organosilane SAMs. Lee at al. demonstrated that charged impurities were more effectively screened by SAM with longer alkyl chain lengths by showing that octadecyl-SAM (C18) resulted in smaller Dirac voltage and higher mobility of graphene than octyl-SAM (C8) [72].

According to a report by Sabri et al., deposition of a thin polymeric layer (a 168 nm film of Parylene-C) on SiO_2 provided the same effect as SAM treatment in terms of reduced hysteresis and enhanced mobility (Figure 4c) [78]. Recently, Shin et al. found that electrical reliability of graphene FETs in an air ambient can be achieved by introducing an ultrathin fluoropolymer to the graphene/SiO_2 interface [79]. With a 7-nm-thick CYTOP fluoropolymer, the carrier density of graphene was changed negligibly even after exposure of the device to an air ambient (RH ~ 45%) for 3 weeks (Figure 4d). A highly hydrophobic buffer such as the fluorinated buffer also contributes to recovery of intrinsic charge neutrality, suppresses hysteresis, and enhances mobility, as mentioned above. It is worth noting that the unique wetting transparency of graphene [80] prevents water molecules from being adsorbed on the graphene surface integrated on the fluoropolymer, resulting in excellent ambient stability of graphene FETs.

Modification of the graphene/target substrate interface by SAM can be also used to tune the carrier type or density, namely doping control, without compromising the intrinsic electrical properties of graphene [81-84]: SAMs terminated with various functional groups induce n- or p-type doping of graphene by charge transfer from a specific functional group or the built-in potential generated from the dipole moment of the SAM. Here, we do not cover this in detail, but readers who are interested in this topic may refer to a recent in-depth review [85]. In connection to this review it should be mentioned that the reported doping levels have shown a wide range of variation in terms of the Dirac point even when the same SAM (for example, aminopropyltriethoxysilane; APTES) was used [84,86-89]. This might be attributable to the integrity of the SAM formed on SiO_2, which sometimes depends sensitively on the chemistry involved in SAM formation such as the treatment methods (phase of SAM during the treatment) and conditions (water content in the ambient atmosphere or solvent) [90]. Hence, more studies are required to exploit SAM doping methods in practical applications beyond academic research based on SiO_2. For instance, given that APTES SAM treatment can provide a more effective and stable n-doping source [87,88] over other doping methods, it is worthwhile to investigate how to achieve a reliable doping level and whether this doping method is also compatible with plastic substrates for the application of APTES SAM to graphene flexible/transparent electrodes. One of the sources of the degradation of the doping strength is the desorption of dopants in chemical doping methods when the doped graphene sample is exposed to the air ambient [91] while the formation of covalent bonding between the SAM and the target substrate can guarantee environmental doping stability.

2.2.2 Substrates with high surface phonon energy

While the passivation of SiO_2 with SAMs or functional polymers is useful to considerably reduce the substrate effects on the electrical characteristics of graphene FETs, the carrier transport in graphene is still limited by thermally excited surface phonons of SAMs or polymers, especially at room temperature. Hence, the combination of

graphene with substrates having high surface phonon energy is the most attractive way to achieve high performance graphene devices operated at room temperature. One outstanding material for this purpose is hexagonal boron nitride (h-BN) [92-98]. h-BN is an insulating isomorph of graphite (Figure 5a), a layered dielectric material with a wide band gap of ~5.97 eV and a dielectric constant of ~4 [92]. A planar, hexagonal lattice structure of the h-BN layer is formed by strong ionic bonding between boron and nitrogen atoms, which provides a chemically inert, dangling-bond-free flat surface [96]. According to Decker et al., these features of the h-BN surface induce lower density of introduced charged impurities in graphene and a considerable reduction of inhomogeneities of charge density in graphene/h-BN, as compared to a SiO_2 substrate (Figure 5b) [97]. Ripples of graphene are also suppressed on h-BN due to its atomically flat surface (Figure 5c) and, even more importantly, the surface phonon energy of h-BN is two times larger than that of SiO_2 [92]. Significant enhancement of the electrical characteristics of graphene devices can hence be expected by the improved interface of the graphene/h-BN system. The highest mobility value reported for CVD-graphene/h-BN is 65 500 cm^2/Vs, which is ~ 30 times higher than that for CVD-graphene/SiO_2 [93].

Wang et al. investigated the effects of graphene/substrate interfaces on the electrical performance of graphene FETs with three different graphene systems: CVD-graphene transferred on SiO_2, CVD-graphene transferred on h-BN flakes, and graphene directly grown on a CVD-h-BN film [98]. The temperature dependence of the graphene resistivity was negligible for graphene/h-BN, indicating that no surface phonons were activated up to room temperature in h-BN due to its high surface phonon energy (Figure 5d). The graphene/h-BN interface thus exhibited superior mobility, a narrower minimum conductivity plateau, and a Dirac point close to zero, as compared to the graphene/SiO_2 interface (Figure 5e). Superb performance of a graphene device was obtained when a graphene/h-BN interface was created by sequential CVD growth of graphene directly on CVD-grown h-BN on Cu due to the absence of residues and adsorbates generated from the transfer process.

While h-BN is an ideal substrate for high performance graphene devices, it is still challenging to synthesize high quality, large area h-BN films. Therefore, from a practical point of view for graphene electronics, it is necessary to develop alternative, cost-effective substrates with high surface phonon energy and with which it is easy to obtain a large sized film with good reproducibility and uniformity. A recent report from Oh et al. demonstrated that aluminum nitride (AlN) substrate can serve as an excellent alternative to h-BN with several of the advantages mentioned above [99]. An ultrathin AlN film with a smooth surface (Rq ~ 0.5 nm) was simply obtained over a large area (4 inch wafer) by a plasma enhanced atomic layer deposition (PE-ALD) method. Top gated graphene FETs on an AlN substrate showed higher mobility than devices on SiO_2, indicating the suppression of surface phonon scattering. The high surface phonon energy of AlN (Table 2) resulted in weaker temperature dependence of mobility (Figure 5f). The RF cut-off frequency was thereby significantly improved in graphene FETs on AlN (115 GHz), compared to those on SiO_2 (55 GHz). Similar enhancement of the cut-off frequency (155 GHz) was also reported by Wu et al. for a graphene FET on diamond-like carbon (DLC) [100], which shows high surface phonon energy (Table 2).

2.3 Interface engineering of graphene/gate dielectric

Integration of graphene with passive components such as gate dielectrics is another important step to achieve high performance graphene devices. Oxide materials with a high dielectric constant (k) have been used as gate dielectrics to fabricate top-gated graphene FETs because high-k dielectrics enable low voltage operation of devices by their high capacitance and also provide scaling capability [101-104]. In conventional electronics, high-k dielectrics have been deposited by atomic layer deposition (ALD), because this technique can produce ultrathin, conformal oxide dielectrics with precisely controlled thickness [105-109]. However, the basal plane of graphene has few dangling bonds [110-113], which are necessary to induce the surface reaction of precursors in the ALD process [114-116]. This unique feature of the graphene surface results in irregular and poor film formation of ALD-dielectrics on pristine graphene [111,113,117]. ALD-dielectrics with a rough surface and many pin-holes cause high leakage current, low breakdown voltage, and extrinsic scattering of charge carriers

Table 2 Material properties of various substrates used in graphene devices

	SiO_2	AlN	BN	DLC	SiC (6H)
Band gap (eV)	8.9	6.28	5.97	1.4	3.05
Dielectric constant	3.9	9.14	5.06	2.5-6	9.7
Crystal structure	Amorphous	Wurtzite	Hexagonal	Amorphous	Hexagonal
Surface phonon energy (meV)	59	83.6	101	<165	116

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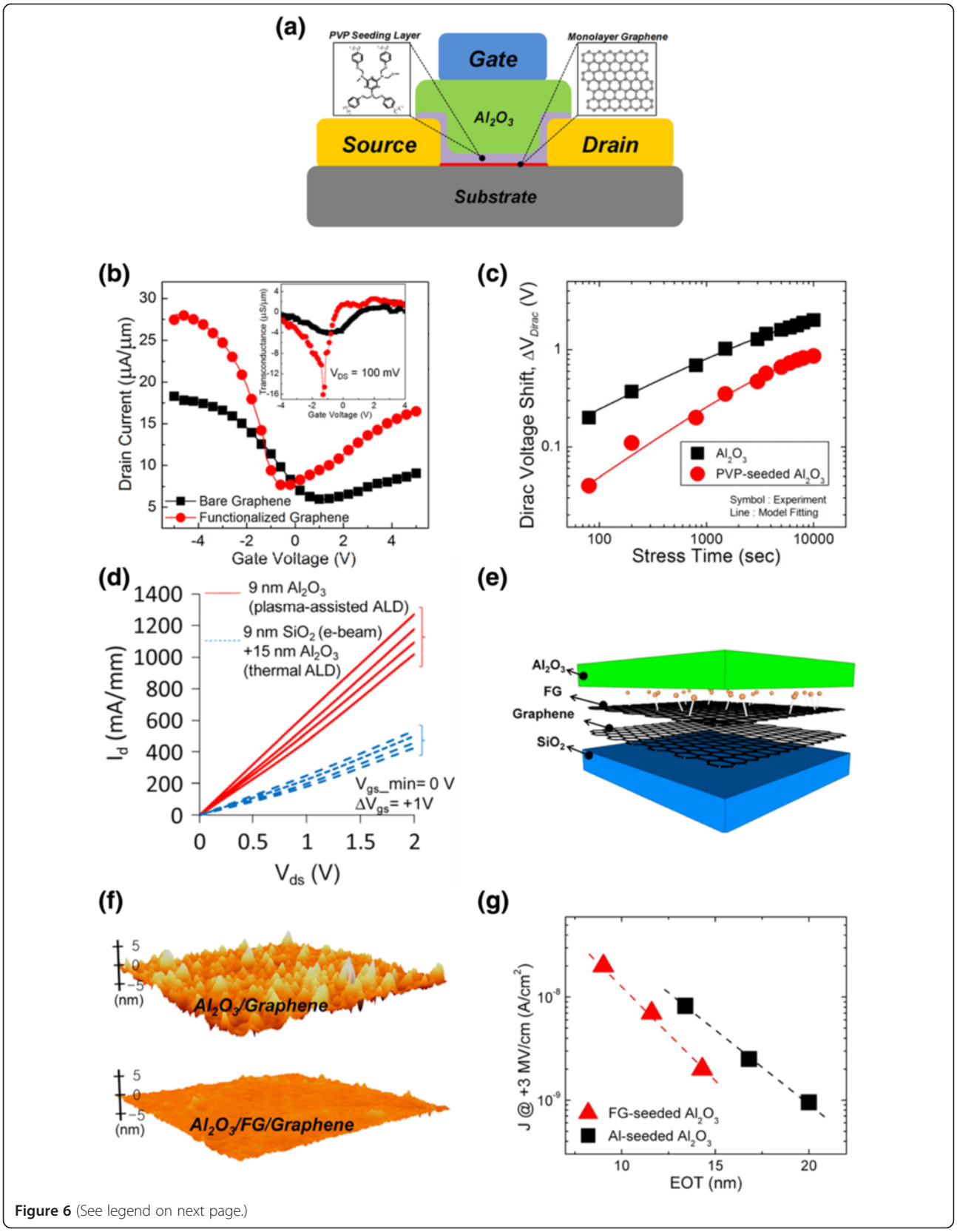

Figure 6 (See legend on next page.)

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Figure 6 Seeding ALD of high-k dielectric on graphene. a, Schematic diagram showing top-gate graphene FET structure with PVP-seeded Al_2O_3 gate dielectric. Reproduced with permission [125]. Copyright 2012, AIP Publishing LLC. **b**, Transfer characteristics (I_d-V_g) of top-gate graphene FET before (black square) and after (red circle) the graphene channel is deposited with PVP. Inset: transconductance of the graphene FETs with different gate dielectrics as a function of gate voltage. Reproduced with permission [125]. Copyright 2012, AIP Publishing LLC. **c**, The time-dependent V_{Dirac} shift of graphene FET before (black square) and after (red circle) the graphene channel is deposited with PVP. Reproduced with permission [125]. Copyright 2012, AIP Publishing LLC. **d**, Output characteristics (I_d-V_d) of transistors based on CVD monolayer graphene with 9nm Al_2O_3 (red line) and 24 nm heterogeneous integrated dielectrics (dashed blue line) via different depositing methods. Reproduced with permission [128]. Copyright 2011, IEEE. **e**, Schematic diagram presenting the functionalized graphene-seeded Al_2O_3 stack on graphene. Reproduced with permission [129]. Copyright 2013, American Chemical Society. **f**, Surface morphology of the Al_2O_3 films deposited on graphene (top) and functionalized graphene (bottom). Scan size: 1×1 μm^2. Reproduced with permission [129]. Copyright 2013, American Chemical Society. **g**, Leakage current densities (at +3 MV/cm^2) versus EOT for dielectrics with functionalized graphene seed layer (red triangle) and Al seed layer (black square) on graphene. Reproduced with permission [129]. Copyright 2013, American Chemical Society.

at the graphene/high-k dielectric interface in graphene FETs. To obtain high quality, uniform high-k dielectrics on graphene, the introduction of seeds on the graphene surface has been proposed as an effective means of fabricating graphene devices using the ALD technique.

2.3.1 Introduction of seeding materials on graphene

Various materials have been used as seeding materials for the formation of uniform, high quality high-k dielectrics on graphene by ALD [113,118-126]. Kim et al. proposed the use of a thin aluminum layer (thickness 1~2 nm) to deposit uniform Al_2O_3 films on graphene [119]. A native aluminum oxide is formed when the thin Al layer is exposed to air, and this oxide provides nucleation sites for the surface reactions during ALD of Al_2O_3. Organic molecules or polymers have been exploited as seeding layers for the integration of dielectrics and graphene [113,122-125]. One example is the use of a poly(vinyl phenol) (PVP) film [125]. Shin et al. prepared an ultrathin, cross-linked PVP seeding layer (thickness ~5 nm) on a graphene surface by a spin-coating method (Figure 6a). Due to abundant functional groups in PVP such as hydroxyl and hydrocarbon, the Al_2O_3 film deposited on the PVP seeding layer by ALD was smooth (R_{rms} ~0.5 nm) without pin-holes. The electrical performance of top-gated graphene FETs was considerably improved with PVP-seeded Al_2O_3, compared to devices with Al_2O_3 deposited on bare graphene. Specifically, the drain current and transconductance were enhanced, resulting in a more than five-fold increase of mobility (Figure 6b). In particular, a graphene FET with PVP-seeded Al_2O_3 showed a suppressed Dirac point shift under a gate bias stress condition (Figure 6c). A recent study by Kim et al. suggested that quantum dot (CdSe) arrays formed on graphene also can serve as a seeding layer for the effective ALD of high-k hafnium oxide on graphene [126].

2.3.2 Functionalization of graphene

To generate seeding sites on graphene, functional groups can be directly introduced to the graphene surface by oxidizing carbon atoms of graphene [112,127-129]. Lee et al. reported on graphene functionalization using ozone (O_3) during ALD of Al_2O_3 [112,127]. An ultrathin (~1 nm), smooth (R_{rms} ~0.1 nm) seed layer was formed on graphene by O_3 treatment in the presence of a trimethylaluminum precursor. Gentle O_3 treatment conditions (at 25°C for 20s) induced negligible defects on graphene while its surface was partially functionalized with epoxide groups. A 15-nm-thick Al_2O_3 layer was uniformly formed by O_3 based ALD, resulting in high performance, top-gated graphene FETs with carrier mobility of 5 000 cm^2/Vs, low V_{dirac} hysteresis, and low leakage current. In the same context, Nayfeh et al. demonstrated that a remote O_2 plasma-assisted ALD technique produced a 9-nm-thick Al_2O_3 layer with better conformal coverage and lower roughness, compared to Al_2O_3 films deposited by thermal ALD [128]. They reported an increase of the defect level in graphene on the basis of Raman measurements, indicating that graphene was functionalized during the O_2 plasma-assisted ALD process. Both drain current and mobility were enhanced in graphene FETs with 9-nm-thick Al_2O_3 by plasma-assisted ALD, compared to those obtained with a 9-nm-thick, e-beam-evaporated SiO_2 interfacial layer plus a 15-nm-thick Al_2O_3 layer by thermal ALD (Figure 6d).

In order to avoid uncontrolled damage of graphene in O_2 plasma or O_3-assisted ALD, Shin et al. proposed a novel approach for reliable high-k dielectric formation on graphene with ALD by introducing an additional functionalized graphene single layer as an ultrathin seed layer on the graphene channel (Figure 6e) [129]. Pristine graphene was transferred to a target substrate and then functionalized (O_2 plasma treated) graphene was stacked on the pristine graphene prior to conducting the ALD process. Al_2O_3 was deposited via conventional thermal ALD on a functionalized graphene layer where the surface

has abundant, oxidized carbon moieties. Al_2O_3 deposited on the functionalized graphene/pristine graphene stack exhibited excellent uniformity with low defect density (Figure 6f; R_{rms} ~0.3 nm). In addition, capacitors with functionalized graphene seeded Al_2O_3 showed lower leakage current density for the same effective oxide thickness (EOT), compared to those with Al-seeded Al_2O_3: this is a considerable advantage of this approach in terms of further scaling of gate oxide thickness (Figure 6g).

3 Conclusions

This review highlighted the importance of interface engineering for high performance graphene devices by considering each interface encountered during the fabrication of graphene devices, from the graphene/metal growth substrate to graphene/high-k gate dielectrics. For effective delamination and transfer of graphene, adhesion at the interface of the graphene/metal growth substrate or graphene/target substrate should be engineered by appropriate weakening or strengthening methods for those interfaces. In terms of graphene delamination using polymer adhesives or a carrier layer, questions remains about which functional groups in the polymer play a critical role to induce delamination of graphene. This should be investigated systematically by applying polymers having various functional groups to graphene delamination systems, in conjunction with an investigation of doping effects that might be induced from the functional groups of polymers.

After graphene is transferred onto a target substrate, interfacial issues arise from the atom-thickness of graphene and the surface-graphene interactions. Since the surface states of substrates significantly affect the overall electrical properties of graphene devices, substrates with a chemically inert, dangling-bond-free flat surface as well as high surface phonon energy are highly demanded. Although h-BN is an ideal substrate in terms of realizing high performance graphene electronics, obtaining reliable, large-area synthesis methods for h-BN beyond mechanical exfoliation is still a challenging issue. On the other hand, alternative substrate materials, such as AlN, are attractive, as highlighted in this review.

To deposit a high-k dielectric using ALD, it is necessary to introduce seed materials onto graphene due to the chemically inert surface of graphene or to generate seeding centers on graphene itself. These approaches cause heterogeneous dielectric stacks (or interfaces) and give rise to difficulty in controlling the film thickness, thereby constraining the scaling of gate dielectric thickness. A novel approach for the deposition of gate dielectrics therefore should be explored to achieve a single component gate dielectric that forms a homogeneous interface without the application of additive seed layers. One example would be the deposition of ultrathin (less than 10 nm) polymer dielectrics by the initiated CVD method, which is under investigation by our group. The use of ultrathin polymer dielectrics in graphene FETs would also be desirable for the development of flexible electronic devices.

Intensive studies in recent decades have provided a great deal of insight into the important role of interface engineering in graphene systems, and have opened up opportunities for the realization of high performance graphene devices. We expect that knowledge accumulated from graphene will be extended to emerging 2D materials for the enhancement and optimization of device performance.

Competing interests

The authors declare that they have no competing interests.

Authors' contributions

DYJ and SYY equally contributed to this work in the manuscript preparation. All authors read and approved the final manuscript.

Acknowledgements

This work was supported by the IT R&D program (10044412), the Global Frontier Research Center for Advanced Soft Electronics (2011–0031640), the Basic Science Research Program (2010–0029132) and Nano-Material Technology Development Program (2012M3A7B4049807).

Received: 11 December 2014 Accepted: 5 January 2015
Published online: 10 June 2015

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